A Wide Dynamic Range Charge Integrating Analog to Digital Converter with FASTCAMAC Readout

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Abstract

The design and performance of a FASTCAMAC gated charge integrating ADC is presented. A high performance charge to time converter (LeCroy MQT300) is coupled with a time digitizer (LeCroy MTD133) to produce a fast converting, wide dynamic range ADC module. The total dynamic range is greater than 17 bits, in three overlapping 12 bit ranges. The smallest LSB is less than 25 fC and the full scale is greater than 6 nC. A sliding scale is implemented in the time domain, to reduce the differential non-linearity of the time digitizer. The dead time is 5.5 microseconds in auto range mode. The FASTCAMAC readout is capable of a maximum rate of 100 nS per ADC measurement (30 Mbytes/sec).

I. INTRODUCTION

The new ADC combines a triple range gated integrator charge to voltage converter, 3 Wilkinson type analog to time converters and a sub nanosecond time digitizer [1]. The result is a high performance, wide dynamic range ADC with low (5.5 µS) dead time.

The ADC is designed as a single width FASTCAMAC module containing 16 ADC channels, with a common GATE. A clear input and a busy output are also provided. The GATE, clear and busy signals are all fast NIM levels, with 50 ohm Lemo style connectors. The 16 inputs are also 50 ohm Lemo style connectors. The sensitivity at the input connector ranges from 25 fC per count on the low (most sensitive) range, to 1.5 pC per count on the high range. Full scale (on the high range) is greater than 6 nC. Each range extends to at least 4096 counts above the pedestal, providing 12 bit resolution on each range.

II. THE DESIGN

A. Overall Design

This new CAMAC ADC module uses two custom monolithic integrated circuits from the LeCroy Corporation. Sixteen LeCroy MQT300a[2,3] triple range gated charge to time converters and two LeCroy MTD133b[4,5,6] eight channel time to digital converters (TDC) form the ADC channels. Control and readout logic is provided by a Xilinx XC4013XL field programmable gate array (FPGA). This is configured on power up from an electrically erasable memory (EEPROM). The EEPROM can be reprogrammed in the field, using normal CAMAC commands, allowing easy upgrades of the firmware. A 24 bit by 1024 FIFO (first in first out) memory is used as the output memory buffer. The FASTCAMAC interface is made with two Xilinx 95108 complex programmable logic devices (CPLD). These CPLDs are also electrically erasable, and can also be reprogrammed in the field using a JTAG connection.

B. Front End and GATE

The NIM GATE signal is converted to emitter coupled logic (ECL) levels and radially distributed to the 16 ADC channels using high speed ECL logic. The 16 input signals are integrated during the GATE interval. The GATE duration can range from 10 nS to 500 nS. The input signals are integrated and converted to a time interval by the LeCroy MQT300a bipolar monolithic integrated circuit. This chip splits the input current into 3 parts in the approximate ratio 64:8:1. Each part is integrated (stored on a capacitor) by an independent (and identical) charge to time converter. At the end of the GATE the charge is removed from the storage capacitor by a 20 µA rundown current. A comparator produces an output signal whose width is the time above threshold of the voltage on the storage capacitor. The time interval between the end of the GATE (when the run down begins) and the trailing edge of the comparator output (when the capacitor voltage returns to its resting value) is the measure of the charge integrated during the GATE.

The basic gain of the MQT300a is 1 nS per 20 fC. The MQT300a requires at least 100 ohm input impedance for best noise performance. In order to provide 50 ohm input impedance at the connector, an impedance matching circuit splits the signal, 2:1, reducing the gain to about 40 fC per nS.

The maximum linear input current at the MQT300a is 50 mA, corresponding to 100 mA (a 5V signal amplitude) at the input connector. The input impedance at the connector is 50 ohms up to 10 V, and about 37 ohms above 10 V, due to clamping circuits that protect the MQT300a.

The outputs of the three charge to time converters are combined with an exclusive OR circuit into one composite signal which is the output to the TDC channel. This signal will have 3 transitions to measure, corresponding to the time over threshold for each of the 3 comparators, one for each range.

The pedestals for the 3 ranges are adjusted so that the high range completes the rundown first, followed by the middle and low ranges. A negative input signal will cause these 3 transitions in the composite signal to spread apart, with the low range being the first to extend beyond the common start time out.

The pedestals must also be initially far enough apart so that small DC offsets of the input signal (which can cause the pedestal to change in either direction) do not cause the transitions to be too close together to be resolved by the TDC (the minimum spacing resolved by the TDC is about 10 nS).

C. Time Digitizer and Sliding Scale

The MQT300a output signal is digitized by the LeCroy MTD133b multi-hit time TDC CMOS integrated circuit. The TDC is operated in common start mode, measuring both positive and negative transitions, with a clock of about 240 MHz. This choice of clock frequency makes the low range gain (at the input connector) about 22 fC per count.

At the end of the GATE a common start signal is generated and sent to the TDCs. An unusual sliding scale circuit is implemented by delaying the application of the common start signal to the TDCs. The delay is generated by 50 ohm controlled impedance strip line delays on the printed circuit board. Four delay lines, about 0.5, 1., 2. and 4. nS provide fifteen steps to delay the common start by up to 9 nS in steps of about 0.5 nS. This step size corresponds to the least count of the TDC with the 240 MHz clock. The 240 MHz clock is generated with a frequency synthesizer on the board, and is easily adjusted (in 1 MHz steps, over a range of 192 to 255 MHz) to match the actual delay line. The prototype printed circuit boards and the first production lot were obtained from different vendors. Although the delays lines were the same length and nominal impedance, the actual delays differed by more than 10% between the 2 sets of boards.

Selection of the delay is accomplished with pairs of 2-input ECL AND gates (in the same package to minimize propagation delay differences).

The TDC is stopped and read out 3.5 µS after the end of the GATE. If a range on a given channel is saturated (the signal is beyond full scale for that range), the transition occurs after the common start time out (more than 3.5µS after the end of the GATE), and is not measured by the TDC. The most sensitive range that is not saturated is identified by counting the number of transitions observed between the common start and the common start time out. The data value for that range is the time of the last transition measured. For example, a 400pC signal will saturate the low range and appear on the middle and high range only. Two transitions will be measured, with the last transition due to the middle range.

The TDC chip has a built in feature, designed specifically for this application, which simplifies the readout and identification of the range. The hits are counted inside the TDC, independently for each channel in a 2 bit counter. This 2 bit value is readout in parallel with the time data for that channel. Also, the TDC can be programmed to read out only one hit for each channel. Since the hits are stored in the TDC in a LIFO (last in, first out), the only hit read is the last hit that was received on that channel.

During readout, the sliding scale delay value is added to the measured time for each channel (the sliding scale delay reduces the measured time, since it delays the common start, not the signal, so it is corrected by adding the delay value). After each event, the delay value is changed, so the final ADC measurements (in a spectrum, for example) are the average over 16 adjacent TDC time bins. This sliding scale effectively eliminates (to below 1%) the differential non linearity (DNL) of the TDC. Note that this sliding scale occurs after the charge to time conversion, and cannot reduce any DNL that comes from the MQT300a.

D. Control logic

The control logic for the module is provided by a Xilinx 4013 FPGA. This CMOS integrated circuit contains nearly all of the low speed (20 and 40 MHz) logic required for this rather complicated module. Only the GATE logic is external, and this requires high speed ECL logic.

The common start signal is detected by the control logic, and the TDCs are stopped about 3.5 µS later (the exact delay depends on the phase of the 20 MHz clock when the GATE ends). After the TDC has been stopped, a 1 µS clear is applied to the MQT300a chips to remove all residual stored charge. Then the TDC is read out at 20 MHz, completing the 16 channels (when in auto range mode) in less than 1 µS. The data flow is pipelined inside the FPGA. During readout several processing steps take place. These are controlled by bits in a control register. Sixteen individual pedestals and sixteen individual sparse scan threshold values (each 12 bits) can be stored in the FPGA. During the processing pipeline the sliding scale delay is added, the pedestal is subtracted, and the data is compared to the sparse scan threshold, in that order. Data which passes the threshold test are stored in the multi event output FIFO buffer. In auto range or sparse mode, the maximum record size is 17 24-bit words, a header and the data from the 16 channels. In all range mode, the event record can be as large as 49 words. The output FIFO buffer can hold 51 (sparse mode) or 19 (all range mode) events. The FIFO memory buffer decouples the readout from the rest of the module, allowing simultaneous readout and data acquisition.

E. CAMAC and FASTCAMAC Interface

The control logic and registers for the CAMAC and FASTCAMAC[7] features are implemented in the FPGA. The CAMAC dataway interface is provided by two Xilinx 95108 CPLDs. These CMOS chips drive the dataway R lines and receive data from the W lines. The CPLD also allows the dataway drivers to be operated as either open collector or CMOS, which allows level 2 FASTCAMAC operation at the maximum rates. During level 2, the readout uses a pipeline register in the CPLD. The S1 and S2 pulse detection is also in the CPLD and uses an external switched delay line (4 steps of 25 nS) to protect against the backplane noise produced during level 2 operation (the data can change at every S1 edge).

The 17 word event record can be read out in 7.4 µs using FASTCAMAC level 1, and in 2.7 µs using FASTCAMAC level 2 at the maximum rate. The readout is independent of the data acquisition, and can proceed simultaneously.

III. PERFORMANCE

A. GATE

This ADC is a gated charge integrating ADC, that is, it integrates the area of the input signal during the GATE. The output of the ADC is directly related to the total charge of the input signal.

The MQT300a operates correctly with GATEs as short as 10 nS, and as long as 500 nS. Longer GATEs are possible, with care to minimize the input offsets. This, coupled with the

large dynamic range, allows the CMC080 to accurately measure signals from fast, high rate plastic scintillators as well as raw signals (no shaping amplifier) from slow scintillators such as Sodium Iodide crystals.

B. Noise and Dynamic Range

With no input signal, and a short GATE (10 nS) the ADC exhibits a noise level of about 1.5 counts RMS on each of the 3 ranges. On the low range (21 fC/cnt) this corresponds to about 33 fC. The noise on the low range increases with GATE width, as shown in Figure 1, to about 60 fC at 500 nS. On the middle and high range, the noise is essentially independent of GATE width, and corresponds to about 0.25 pC and 2 pC, respectively.
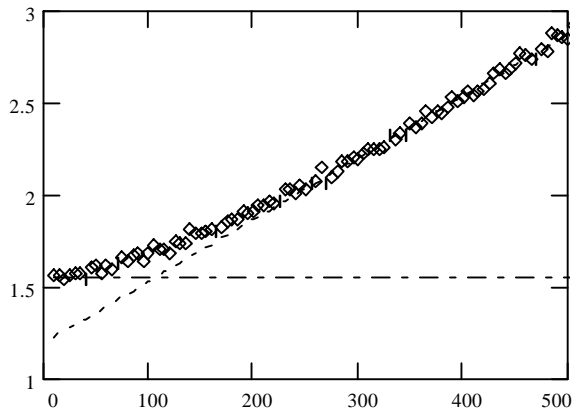
Figure 1. The average (of all 16 channels) RMS noise (in counts) on the most sensitive range, as a functiion of GATE width in nanoseconds.

The pedestal, maximum count, gain and full scale for each range is shown in table 1, for a typical channel. The high range actually extends to 6800 counts (6800 counts corresponds to 3.5 μs with the 240 MHz clock), which is beyond the range of the DAC used in this test setup. Although the pedestals may appear excessively large, recall that they can be subtracted during readout. The full scale value in the table is the gain times 4096. The actual full scale (when the range changes) can be nearly 50% larger

Table 1
Typical ADC Channel Pedestal, Gain and Full Scale (4096 cnts).

Range	Pedestal counts	Full Scale counts	Gain PC per cnt	Full Scale pC
Low	1854	6800	0.0211	>86.
Middle	1448	6800	0.164	>672.
High	903	6800	1.31	>5,366.

The gain of the MQT300a is determined by currents, which are set by external resistors and voltages. As a result the channel to channel gain variation is small, typically less than 3% RMS. The range to range gain is determined by the sizes of transistors in the MQT300a, and also shows a variation less than a few percent. The relative gains (low to mid and mid to high) for the 3 ranges on each channel are easily measured by operating in all range mode, which reads out all transitions for each channel, not just the last one. In this mode the same signal is effectively measured simultaneously on all 3 ranges.
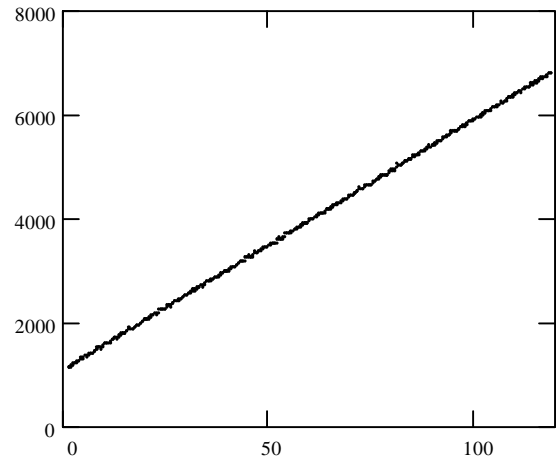
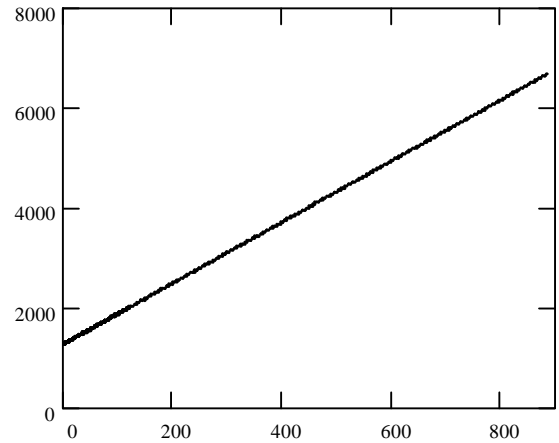Figure 2a. ADC counts (ordinate) vs input charge in pC (abcissa), for low range.

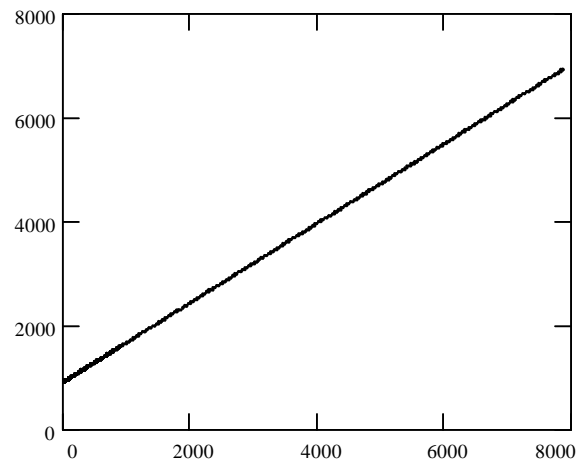Figure 2b. ADC counts (ordinate) vs input charge in pC (abcissa), for middle range.

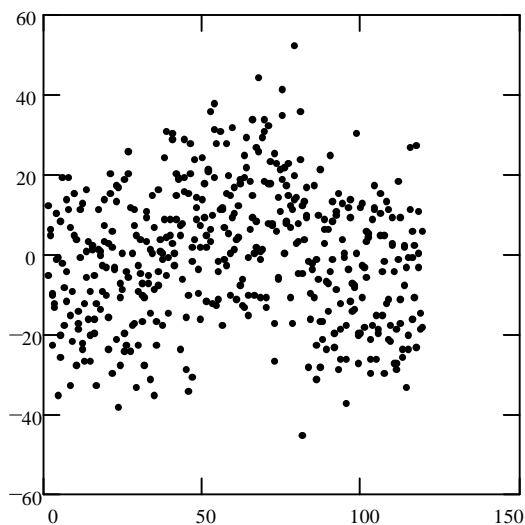Figure 2c. ADC counts (ordinate) vs input charge in pC (abcissa), for high range.

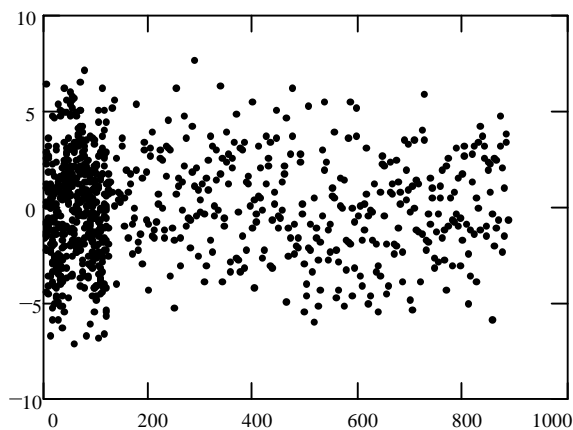Figure 3a. Residual in counts (ordinate) vs input charge in pC (abcissa), for low range.

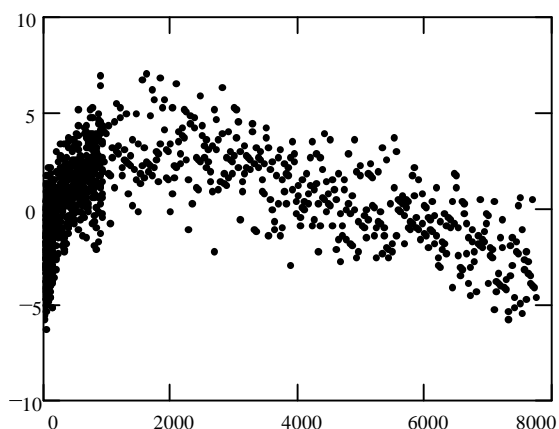Figure 3b. Residual in counts (ordinate) vs input charge in pC (abcissa), for middle range.

Figure 3c. Residual in counts (ordinate) vs input charge in pC (abcissa), for high range.

The TDC count versus input signal (for the same channel as Table 1) is shown in figure 2, for the 3 overlapping ranges. These measurements were made by supplying a variable DC signal to the input with a 16 bit DAC and applying a 500 nS wide GATE signal. With this GATE width, a 1 Volt input signal from the DAC corresponds to approximately full scale.

C. Linearity

The integral linearity was measured by fitting a straight line to the data of figure 2, and plotting the residuals. These are shown in figure 3, for the three ranges. The random spread in the residuals is due to noise, both ADC noise and DAC noise. The only significant departure from linearity is on the high range, and is about 0.1% of full scale.
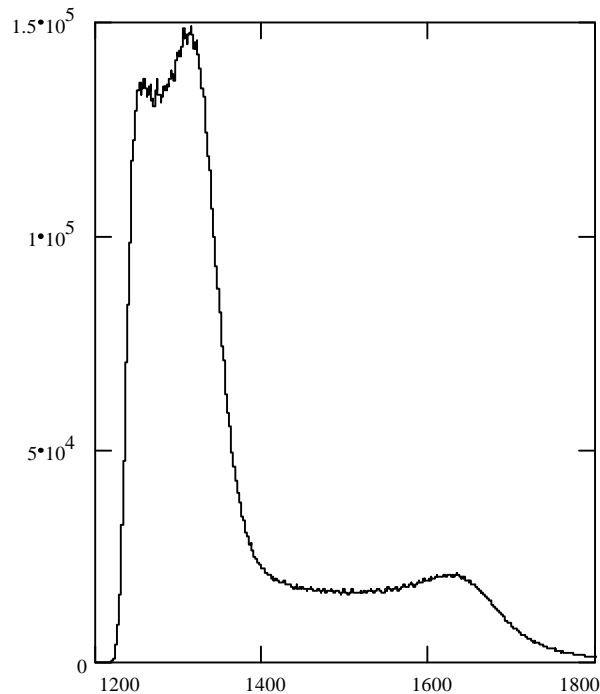

Figure 4. Histogram of a Na22 spectrum, taken with the CMC080, using a photomultiplier and plastic scintillator. Thhe abcissa is the ADC value in counts, (middle range), and the ordinate is the number of counts in that channel.

The differential non linearity has also been measured, using a Na22 source a Hamamatsu R6900U photomultiplier and a 4x4x3 cm. Plastic scintillator. This produced random pulses, random both in amplitude and time. The complete spectrum is shown in Figure 4, and an enlargement of a small part of the central (nearly flat) portion is shown in Figure 5.

The contribution from the TDC has been almost entirely suppressed by the sliding scale. The remaining DNL (typcally less than 1% RMS) is the same on all 3 ranges of the ADC. It is synchronous with the TDC clock, and appears to be due to coupling of the 240 MHz clock into the QVT300a. This was observed in the first prototypes, and much effort has gone into understanding and reducing the coupling. The production board improved the separation of the power and ground between the QVT300a and the MTD133b, and even inserted active buffers between the ECL outputs of the QVT and the MTD inputs. Alas, the DNL is about the same as the prototype!

However, note that for spectra with less than a few thousand counts per channel, the ADC is completely statistics

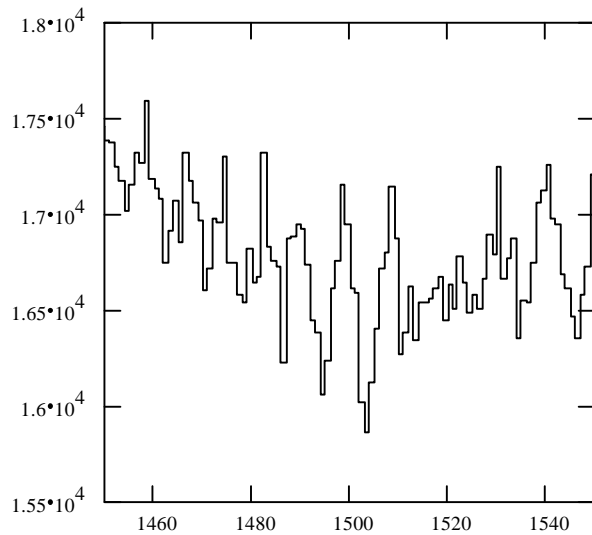limited, and exhibits no DNL. Reducing this DNL is a continuing effort.

Figure 5. Enlargement of a small portion of Figure 3. Note the suppressed zero on both axes. The residual DNL is clearly visible. The DNL has a period of 8 counts, corresponding to the 240 MHz TDC clock.

IV. SUMMARY

A new FASTCAMAC ADC module [8] has been described, with emphasis on its front end and readout. This module is a high performance FASTCAMAC module and is expected to help resolve the FASTCAMAC chicken and egg problem. There are no FASTCAMAC level 2 controllers because there are no FASTCAMAC level 2 modules, and vice versa!

V. ACKNOWLEDGMENTS

This ADC uses a new LeCroy integrated circuit, which was developed primarily as a component for two large physics experiments, and has not previously been used in a commercial module. We have drawn heavily on the designers of the chip, Keith Roberts and Brian Yamrone, both at LeCroy, and thank them for their patience and insights.

VI. REFERENCES

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